

Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

Claim Amendment

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

Claims 1-12 (cancelled)

Claims 13-24 (cancelled)

25. (new) A three-dimensional memory structure, comprising:

a first stack line, having:

a first first-type polysilicon layer;

a second first-type polysilicon layer;

a first conductive layer between the first first-type polysilicon layer and the second first-type polysilicon layer; and

a first anti-fuse between the first first-type polysilicon layer and the second first-type polysilicon layer; and

a second stack line crossing over the first stacked line, having:

a first second-type polysilicon layer;

a second second-type polysilicon layer;

a second conductive layer between the first second-type polysilicon layer and the second second-type polysilicon layer; and

BEST AVAILABLE COPY

Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

a second anti-fuse between the first second-type polysilicon layer and the second second-type polysilicon layer.

26. (new) The memory structure of claim 25, wherein the first-type polysilicon layer comprises an n-type polysilicon layer.

27. (new) The memory structure of claim 26, wherein the second-type polysilicon layer comprises a p-type polysilicon layer.

28. (new) The memory structure of claim 25, wherein the first-type polysilicon layer comprises a p-type polysilicon layer.

29. (new) The memory structure of claim 28, wherein the second-type polysilicon layer comprises an n-type polysilicon layer.

30. (new) The memory structure of claim 25, wherein a material of the first anti-fuse and the second anti-fuse comprises oxide.

31. (new) The memory structure of claim 25, wherein a material of the first conductive layer comprises tungsten silicide.

Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

32. (new) The memory structure of claim 25, wherein a material of the second conductive layer comprises tungsten silicide.

33. (new) The memory structure of claim 25, wherein a material of the first conductive layer comprises titanium silicide.

34. (new) The memory structure of claim 25, wherein a material of the second conductive layer comprises titanium silicide.

35. (new) A three-dimensional memory structure, comprising:
a plurality of first stack lines, wherein each first stack line comprises:
an upper first-type polysilicon layer;
a lower first-type polysilicon layer;
a first conductive layer between the upper and the lower first-type polysilicon layers; and
a first anti-fuse between the upper first-type polysilicon layer and the lower first-type polysilicon layer;
a first dielectric layer in a space between the first stack lines;

Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

a plurality of second stack lines crossing over the plurality of the first stack lines, wherein a pattern of the upper first-type polysilicon layer is substantially conformal to a shape of an interaction between each second stack line and each first stack line, wherein each second stack line comprises:

- an upper second-type polysilicon layer;
- a lower second-type polysilicon layer;
- a second conductive layer between the upper second-type polysilicon layer and the lower second-type polysilicon layer; and
- a second anti-fuse between the upper second-type polysilicon layer and the lower second-type polysilicon layer; and
- a second dielectric layer in a space between the second stack lines.

36. (new) The memory structure of claim 35, wherein the first anti-fuse comprises an oxide material.

37. (new) The memory structure of claim 35, wherein the second anti-fuse comprises an oxide material.

Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

38. (new) The memory structure of claim 35, wherein while the first-type polysilicon layer comprises a p-type polysilicon layer, the second-type polysilicon layer comprises an n-type polysilicon layer.

39. (new) The memory structure of claim 35, wherein while the first-type polysilicon layer comprises an n-type polysilicon layer, the second-type polysilicon layer comprises a p-type polysilicon layer.

40. (new) A three-dimensional memory structure, comprising:

a plurality of first stack lines, wherein each first stacked line comprises:

a first upper first-type polysilicon layer;

a first lower first-type polysilicon layer;

a first conductive layer between the upper and the lower first-type polysilicon layers; and

a first anti-fuse between the first upper first-type polysilicon layer and the first lower first-type polysilicon layer;

a first dielectric layer in a space between the first stack lines;

a plurality of second stack lines crossing over the plurality of the first stack lines,

wherein a pattern of the upper first-type polysilicon layer is substantially conformal to a

Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

shape of an interaction between each second stacked line and each first stacked line,
wherein each second stack line comprises:

- an upper second-type polysilicon layer;
- a lower second-type polysilicon layer;
- a second conductive layer between the upper and the lower second-type polysilicon layers; and
- a second anti-fuse between the upper and the lower second-type polysilicon layers;
- a second dielectric layer in a space between the second stacked lines;
- a plurality of third stacked lines crossing over the plurality of the second stacked lines, wherein a pattern of the upper second-type polysilicon layer is substantially conformal to a shape of an interaction between each third stack line and each first stack line, and wherein each third stack line comprises:

- a second upper first-type polysilicon layer;
- a second lower first-type polysilicon layer;
- a third conductive layer between the second upper and the second lower first-type polysilicon layers; and
- a third anti-fuse between the second upper first-type polysilicon layer and the second lower first-type polysilicon layer;
- a third dielectric layer in a space between the third stacked lines; and

Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

at least a plug in the second dielectric layer connecting the first conductive layer and the second lower first-type polysilicon layer.

41. (new) The three-dimensional memory structure, wherein the plug comprises polysilicon plug.

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.